Silicon-Based Reconfigurable Antennas—Concepts, Analysis, Implementation, and Feasibility

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***Abstract*—We report on an innovative reconfigurable antenna concept with significant practical relevance based on the dynamic definition of metal-like conductive plasma channels in high-resistivity silicon that are activated by the injection of dc current. The plasma channels are precisely formed and addressed using current high-resolution silicon fabrication technology. These dynamically defined plasma-reconfigurable antennas enable frequency hopping, beam shaping, and steering without the complexity of RF feed structures. This concept shows promise for delivering the performance and capabilities of a phased array, but at a reduced cost. However, challenges such as p-i-n biasing circuit complexity and their nonlinearities, as well as antenna efficiency, would still require further investigations.**

***Index Terms*—Holographic antennas, plasma antennas, reconfigurable antennas, silicon, SPIN devices.**

I. Background

THE last several years have seen an exponential growth in the development of *reconfigurable* antennas, i.e., antennas whose aperture can be dynamically modified to enable different functions at different times. The antenna aperture can be specifically tailored to the application at hand, greatly increasing antenna efficiency and signal-processing speed, while maintaining a high degree of flexibility. The development efforts include real-time or even partial reconfigurability using either semiconductor or microelectromechanical switches (MEMS). For example, Chang *et al.* [1] utilized p-i-n diode switches to reconfigure a leaky mode patch antenna.

Along these lines, we have developed an exciting and innovative approach based on silicon technology to implement dynamic antenna aperture reconfiguration. It is based on using lateral p-i-n devices as conductive radiating elements in a **REC**onfigurable **AP**erture (RECAP) [2]. p-i-n devices act as plasma islands when injected by carriers, thus allowing full control on form, shape, and function of these plasma metallic-like radiators [3]. This approach generally leads to a high level of reconfiguration flexibility and numerous attainable configurations. They can be used to reconfigure, hop, shape, and steer the antenna radiation pattern.

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Antenna functionality depends on the antenna's radiating elements' parameters, such as the sizes, shapes, and positions of the radiating elements over the aperture. Modifying (i.e., reconfiguring) the parameters of these radiating elements enables using the same antenna aperture for multiple functions [4]–[10]. For example, the conventional method to achieve reconfigurability is to allow reconnectivity between the various predefined conducting regions, using multiple switches to change the size or shape of the antenna aperture. In our approach, there are no predefined conductive patterns, only well-defined channels on the **S**urface of the high resistivity silicon wafer. Lateral **p-i-n** devices are the basic building blocks of these channels (**SPIN** devices), which are optimized to achieve a relatively high conductivity (10^{18} carrier/cm^3) that is near that of a metal, under dc control [11]. Injection of dc current into a SPIN device will create carriers in the intrinsic region (I-region), which will appear to be metal-like and conductive at RF frequencies. The conductivity of the surface p-i-n devices depends on a number of factors, including the carrier lifetime, carrier concentration, and channel depth.

Our approach is based on semiconductor (i.e., silicon) processing technology. Silicon technology was selected to develop these SPIN devices to create well-defined plasma channels, as high resolution is easily achieved today utilizing lithographic technology on silicon. We have developed novel processing techniques to achieve high-performance high-yield lateral p-i-n devices. The developed process in silicon also has the potential for low-cost mass production, and high degree of integration as dc feed lines, control circuitry, and even RF-feed can be part of the developed antennas.

This innovative plasma concept can enable a truly reconfigurable aperture, rather than the conventional switchable configurations that use multiple switches. For comparison and illustration, Fig. 1 shows a conventional reconfigurable copper dipole antenna, and a similar one made of plasma. The conventional reconfigurable dipole will use the multiplicity of switches to change the dipole length, whereas the plasma approach dynamically defines the dipole shape and length using SPIN devices with dc control.

We have proposed the configuration shown in Fig. 2 for implementing reconfigurable antennas. The antenna comprises an active semiconductor (silicon) layer, on which an x-y grid of SPIN devices is formed. These diodes are addressable by an integrated control circuitry located at the back of the radiating aperture. The dc-bias lines are feed-through p-i-n's that are part

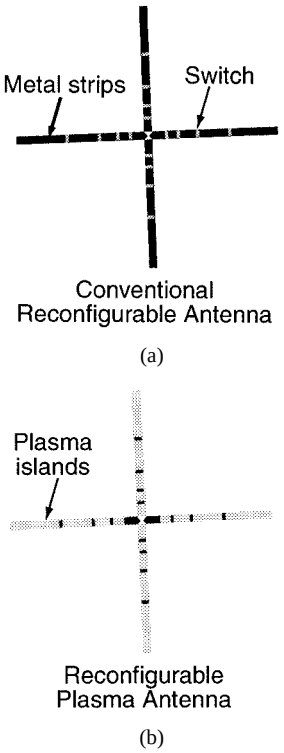

Fig. 1. Reconfigurable dipoles. (a) Metal strips connected/isolated using (MEMS or p-i-n) switches. (b) Plasma islands are activated or deactivated to reconfigure the dipole.

of the RF multilayer structure. Meanwhile, the x-y grid and dc control approach allows precise definition of plasma channels. The locations and shapes of these defined channels can be precisely addressed over the whole processed silicon wafer, using less power in comparison to the optically controlled channels [4]–[10].

This concept of antenna reconfigurability can be extended to include reconfiguring a structure, tweaking an existing one, or allowing frequency hopping. The grid (shown in Fig. 2) under dc control can be dynamically reconfigured, for example, to "paint" various novel antenna structures. Wired antennas are good examples for reconfigurability demonstration because we can define wired elements such as dipoles, folded dipoles, bow ties, and Yagi antennas. Meanwhile, antennas such as patches or any other surface-type antennas can be defined using a mesh-type structure. Fig. 3 shows various forms of these antennas, including a holographic antenna [12], [13]. It is important here to recognize that there is always a need for RF feed. In the case of a wired antenna, for example, the RF feed is a fixed one, and for a holographic antenna, it can be either an integrated feed or space feed (see Figs. 2 and 3). In the following sections, we will describe the SPIN device development efforts and the various validation experiments to prove the feasibility of this approach.

We have also developed mathematical models for calculating the holographic fringes required for generating a given far-field pattern. The developed schemes include multibeam and antenna steering. The algorithm complexity required for setting various holograms will depend on the desired array flexibility. For preset-scan patterns, beam lookup tables would

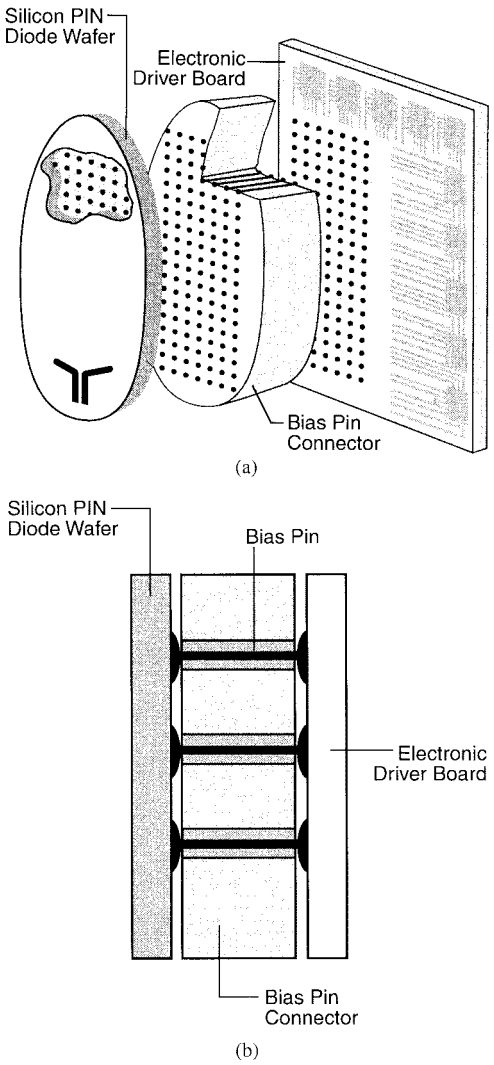

Fig. 2. (a) Plasma grid structure is fabricated on the top of the silicon wafer using SPIN devices; there is an integrated feed, dc circuitry and control as well. Bias p-i-n's are used for bias connectivity (integrated feed). (b) Cross section of the plasma grid structure illustrating layer interconnection.

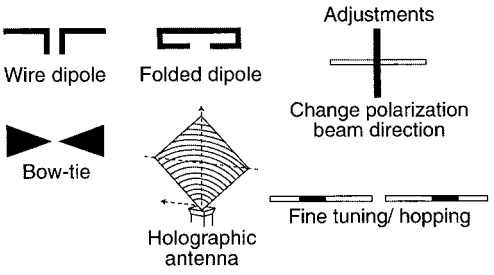

Fig. 3. Various wired antenna configurations that can be implemented using the grid structure. The configurations include dipole, folded dipole, bow tie, and holographic antenna fed by a horn (space-fed). The same concept can be used for polarization control and frequency hopping.

suffice, for example. However, for a real-time scan with varying beam-shape characteristics, these calculations would have to be performed "on the fly." A more rigorous analysis of the holographic antennas including excitation has been also carried out [13] using electromagnetic simulation.

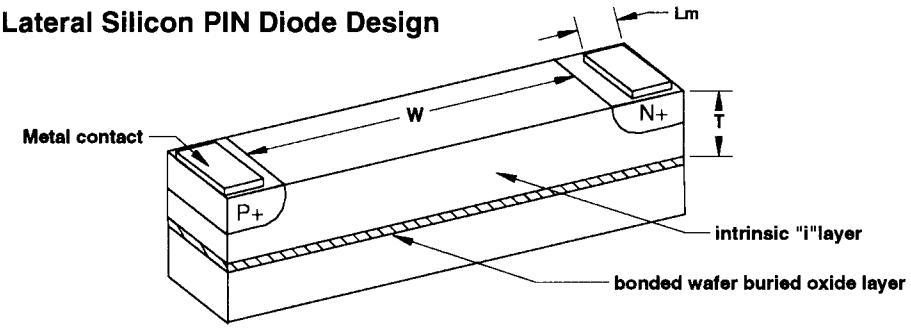

Fig. 4. Structure of lateral p-i-n diode device, length of the intrinsic I-layer $= W$, its depth $= T$, length of the metal contact pad $= L_m$, a thin oxide layer is used to bond the SPIN device to a silicon wafer or other substrate layers.

II. SPIN Device Development

The principle of the reconfigurable antenna is based on surface p-i-n devices as radiating elements. The low resistance of a p-i-n device biased in the forward direction depends on the carrier lifetime of the device. A high carrier lifetime can be easily achieved when using high-resistivity silicon wafers [14]. Hence, SPIN devices are fabricated on high-resistivity silicon. From the RF point-of-view, a multilayer structure is needed to prevent moding and excessive RF losses [13] where the very thin high-resistivity silicon layer is one of this multilayer structure. In addition, we use silicon for several reasons, i.e., large size, the easy availability of low-cost high-quality silicon wafers, and their excellent mechanical strength and high thermal conductivity relative to other semiconductor materials. The carrier lifetime in high-resistivity silicon devices is also high. These factors favor silicon as a low-cost high-yield device material.

Since the SPIN devices are not used as a classical p-i-n diode microwave switch, their layout is significantly different from the standard microwave device. The traditional monolithic p-i-n diode [15] is a vertical device, where the central "intrinsic or low doped" layer is stacked between heavily doped N^+ and P^+ layers. The "I" layer dimensions are selected based on the OFF state isolation, reverse breakdown voltage, and switching speed goals. A cylindrical-shaped mesa-etched device is common for discrete devices, with a thermal oxide to passivate the exposed sidewall silicon to reduce surface trapping and maintain high breakdown characteristics.

Our application requires quite a different structure. The device must be lateral, with the "I" layer fully exposed from the top of the wafer. The SPIN device is required to provide a long "I" layer, where the injection of carriers under forward bias creates a steady-state plasma of free carriers. This region of highly mobile charges then mimics the electrical performance of a metallic conductor. In the OFF state, we want the "I" layer to exhibit high resistance and have small parasitic capacitive coupling between contacts, but the reverse breakdown voltage and switching speed are not first-order concerns. It is desirable to make the metal contacts joining adjacent diodes as narrow as possible. For this application, to minimize the drive current and thermal dissipation within the device, a good device should confine the carriers to be close to the top surface of the wafer and have long carrier lifetime. Ultimately, if a two-dimensional (2-D) diode grid is used to "paint" new antenna configurations, lateral isolation between devices is also required.

Fig. 4 illustrates the SPIN device structure. This is an extremely simple semiconductor device. It requires only N^+ and P^+ regions and metal contacts to connect adjacent devices [16], [17]. The SPIN device process is not complicated, using only 5–6 photomask layers. The design rules are very relaxed, with 3 μm as the smallest feature size. All fabrication steps are compatible with processing on a standard silicon line. The lot processing cycle time is short, and should provide very high yield with low cost.

In the SPIN device, the carriers are confined to the top surface. The device dimensions, doping concentrations, and boundary layers are optimized to trap carriers in well-defined channels approaching high concentration levels exceeding $10^{18}/\text{cm}^3$ with minimal dc drive current. The thickness of these plasma islands is within 2–3 skin depths, and separated from the device body by an oxide layer [17], [18]. Also, lateral isolation between neighboring devices can be enhanced by using trenches [17] (see Table I for the device design approach).

Our application requires the SPIN device or channel to be conductive. As stated, conductivity, which is function of carrier lifetime, is achieved by the high concentration of carriers near the aperture surface. The carrier lifetime, as a function of device layout and process variations, can be easily assessed by measuring the device's forward-bias resistance, and by observing the recovery transient time constants in returning to the OFF-state condition. Based on published experimental results [18], carrier lifetimes in excess of 5 μs are possible. The carrier diffusion length is the square root of the product of carrier lifetime and the diffusion constant (estimated at 35 cm^2/s). This leads to an estimate for the length of the "I" layer to be in the range of 100–200 μm. To emulate a metallic conductor with silicon, the density of injected carriers must be very high, in the range of 10^{18}–10^{19} per cm^3. For a 50-μm-wide device, this level of plasma density can be achieved at a current level of 20 mA. For a plasma density of approximately 10^{18} carriers/cm^3, a layer that is a three-skin depth is approximately 30–50 μm (within our operating frequency range) in thickness. By effectively confining the vertical and lateral dimensions of the conducting channel, the drive current and, hence, power requirements and thermal load on the structure, can be minimized. Vertical confinement

TABLE I
SILICON SPIN DEVICE DESIGN APPROACH

Requirement	Design Approach
Injected carrier density >10^{18} per cm^3 Injected carrier plasma extends across I	Make the length of the intrinsic layer (**W**) =100-200μm
Minimize required drive current	Reduce the active region thickness (**T**) - Chemically etch to thin substrate - Use bonded wafer with buried oxide for isolation
Make device disappear in OFF state	Make metal contact length ($\mathbf{L_m}$)<< length of the intrinsic I region (**W**)
Lateral isolation between devices	(Spacing >recombination length) for spatial resolution

is achieved with the buried oxide layer of a bonded wafer substrate.

We have performed a series of simulations to gain insight into the optimal configuration of the lateral SPIN device. Our basic physics and assumptions were as follows.

1) The carrier hole and electron densities are equal, i.e., $p = n$. Since the carrier densities are high and of the same amplitude, ambipolar diffusion "D_a" will dominate, due to carrier-carrier scattering, i.e., $D_a \approx 16/\sqrt{1+(n/10^{17})}$.
2) Hole current ($J = J_p$) dominates at the P-I contact and electron current dominates ($J = J_n$) at the N-I contact. Since J_p is zero at the N-I contact, the holes create a built-in field that aids the electron flow. Thus, at the contact, $J = 2qDdn/dx|_{x=-w/2}$, where q is electron charge and D is the diffusion constant.
3) Surface recombination at sidewalls and Auger recombination (three carrier interactions) in the bulk must be considered. Also, under steady state, the diffusion equation becomes

$$\frac{\nabla D_a(n)\nabla n - n}{\tau - \gamma n^3} = 0 \tag{1}$$

where γ is the Auger coefficient and τ is the carrier lifetime.

One-Dimensional (1-D) Analysis: Ambipolar diffusion and Auger recombination limit the diffusion length of the intrinsic region of the p-i-n diode because both the ambipolar diffusion constant and effective lifetime decrease dramatically with carrier density. We can describe this effect by defining an effective diffusion length, $L_e = \sqrt{D_a(1/\tau_a + \gamma n^2)}$. The Auger coefficient is $\gamma = 2 \times 10^{-31}$ cm^6/s and we assume a large minority carrier lifetime $\tau_a = 200$ μs. Table II demonstrates the dramatic reduction in effective diffusion length as carrier density increases.

1-D Numerical Solution: We have computed a 1-D numerical solution to the nonlinear partial differential equation (PDE) to demonstrate the behavior of the carriers under the best of circumstances, i.e., when the contact extends from one side to the next (100% fill factor), and the surface recombination velocity at the sidewalls is zero (no surface recombination).

We first reformulate the equations to simplify applying MATLAB's ordinary differential equation solver to the problem. We normalize the x-direction to the low-level diffusion length $L_e = L_o$ by neglecting Auger recombination and using the maximum value of the ambipolar diffusion constant 16 cm^2/s. We obtain $L_o = 564$ μm, normalize the I-region half-width to L_o so that $d = W/2L_o$, and normalize the carriers to some reference level n_R. A convenient level is that where the ambipolar diffusion constant begins to drop, e.g., $n_R = 10^{17}$ cm^{-3}. We define $K = \gamma\tau_a n_R^2 = 0.4$. We define the normalized current j, $j = JL_o/2qD_n n_R$, and the asymmetry constant $B = (\mu_n - \mu_p)/(\mu_n - \mu_p)$. Equation (2) shows the resulting boundary condition problem, and (2) is solved numerically using MATLAB function bvp4c, which is a finite-difference code that implements the three-stage Lobatto IIIa formula. This is a collocation formula and the collocation polynomial provides a C1-continuous solution that is fourth-order accurate uniformly in the interval. Mesh selection and

$$\begin{aligned} y_1' &= y_2\sqrt{1+|y_1|} \\ y_2' &= y_1\sqrt{1+Ky_1^2} \\ y_2(-d) &= j \\ y_2(d) &= -Bj \end{aligned} \tag{2}$$

error control are based on the residual of the continuous solution.

TABLE II
DRAMATIC REDUCTION IN EFFECTIVE DIFFUSION LENGTH AS CARRIER DENSITY INCREASES

n (carrier density)	L_e(μm) (carrier effective diffusion length)
10^{16}	564.6
10^{17}	402
10^{18}	48.5
2x10^{18}	20.8
5x10^{18}	6.7
10^{19}	2.2

Fig. 5(a)–(d) shows the results for normalized current $j = [1, 2, 5, 10, 20, 50, 100, 200]$ from the bottom curve to the top one. The three sets of curves labeled n/n_R versus distance show the electron density in the intrinsic region. They demonstrate that the length of the intrinsic region must be approximately 100 μm to reach a carrier density of 10^{18} per cm^3 or better ($n/n_R \geq 10$) throughout the region without having too high a carrier density adjacent to the contacts. In general, we do not want to drive the device into extremely high injection regimes because the high carrier density will cause significant injection back into the contact regions, causing an additional contribution

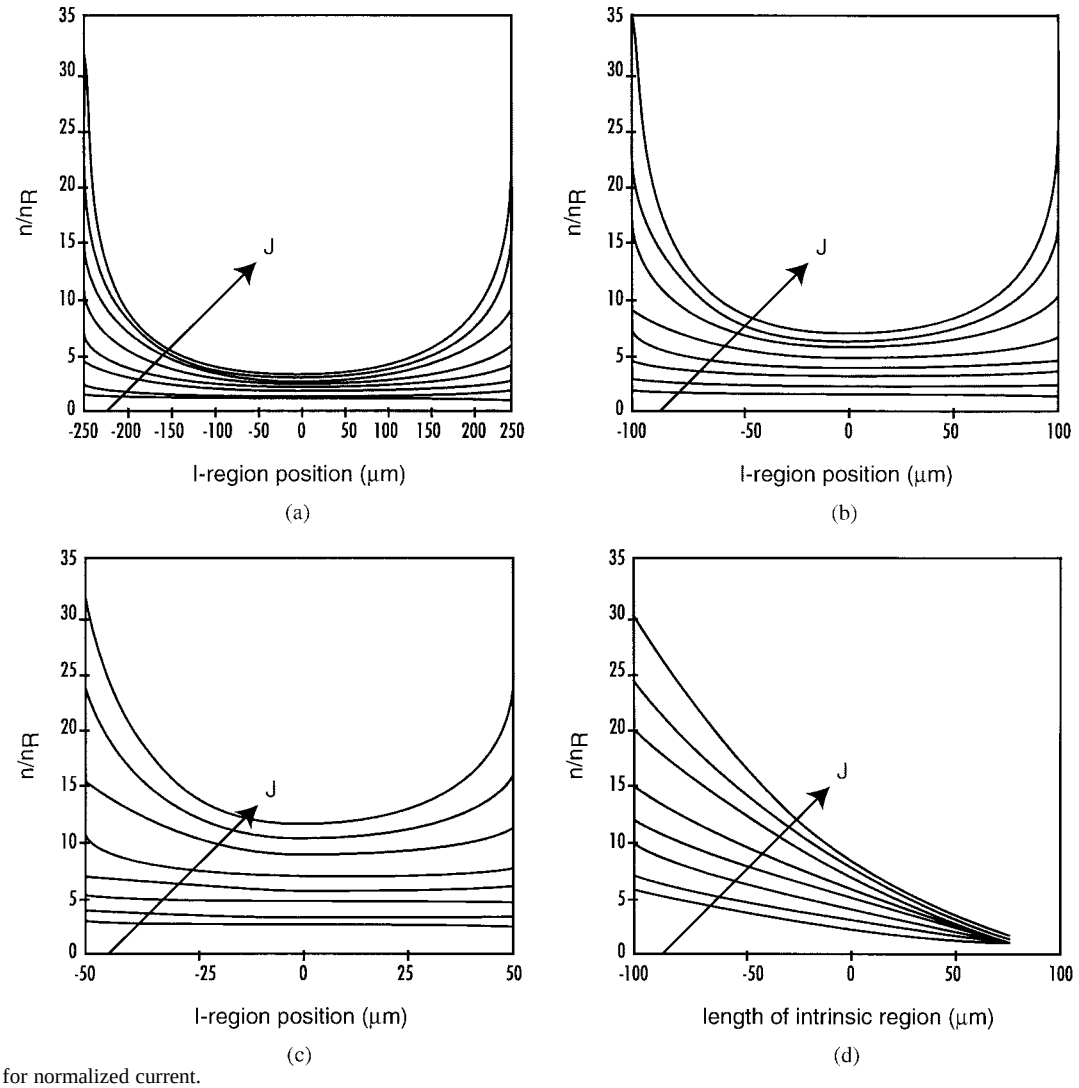

Fig. 5. Results for normalized current.

to current flow. This additional contribution due to diffusion current in the contact regions does not add to the carrier density in the intrinsic region, but adds significantly to power dissipation.

2-D Numerical Solution: The 1-D results indicate a minimum design criterion. However, carrier spreading and sidewall recombination must also be considered since both effects reduce the average carrier density. Therefore, we use 2-D analysis to estimate the impact of these phenomena.

The following equation (3) is the nonlinear PDE describing carrier distributions in the intrinsic region of a p-i-n diode under high injection:

$$\nabla \frac{1}{\sqrt{1+|u|}} \nabla u - u - Ku^3 = 0. \tag{3}$$

We transform this equation into normal form, $\nabla^2 t = f(t)$ through the substitution $u = (t+2)^2/4 - 1$ so that $f(t) = (t^2/4 + t) + K(t^2/4 + t)^3$. We discretize the equation using Newton's method to obtain $Lu^{(k+1)} - f'[u^{(k)}]u^{(k+1)} = f[u^{(k)}] - u^{(k)} f'[u^{(k)}]$. We then numerically solve the PDE using successive over relaxation.

A program was written in MATLAB's script language to perform this calculation. Several examples of the results are shown below.

Case I: Reflecting Sidewalls: Fig. 6 is characterized by I-region length $= 100\ \mu$m, diode width $= 200\ \mu$m, and contact width $= 100\ \mu$m. By comparing the 1-D solution to the 2-D solution along the center of the diode ($y = 0$), we can estimate the effect of carrier spreading. In the case of reflecting sidewalls, there is a small reduction ($\sim 5\%$) in the carrier density at the center.

Case II: Absorbing Sidewalls: Fig. 7 is characterized by I-region length $= 100\ \mu$m, diode width $= 200\ \mu$m, and contact width $= 100\ \mu$m. In this case, the surface recombination velocity at the sidewalls is sufficiently high that we assume that the carrier density goes to zero. This is the worst case. The first thing we notice is that the minimum carrier density has been reduced by approximately 15%, in contrast to the previous case. This can be interpreted as a portion of the applied current going into lateral flow (opposing directions for the two carriers) and not contributing to forming the steady-state carrier density. This effect is magnified for narrow devices, as shown in Case III.

Case III: Absorbing Sidewalls, Narrow Device: Fig. 8 below is characterized by I-region length $= 100\ \mu$m, diode width $= 50\ \mu$m, and contact width $= 50\ \mu$m. Note the significant reduc-

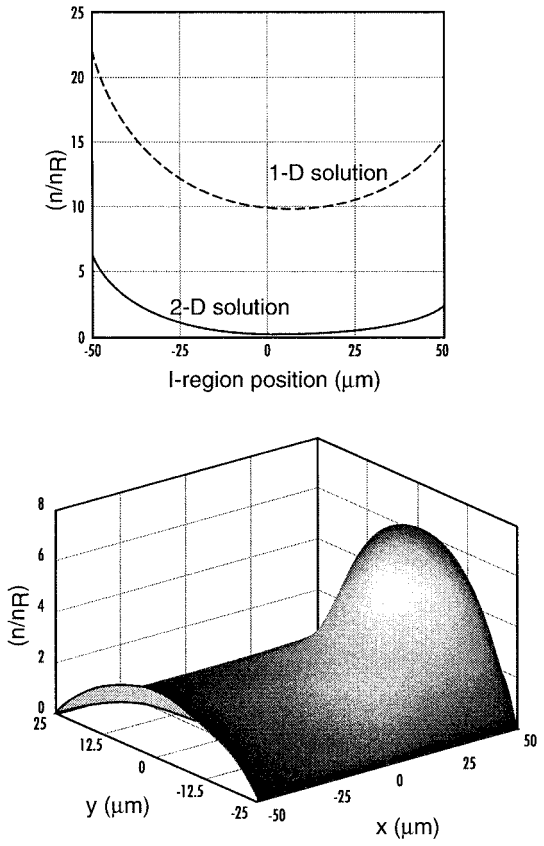

Fig. 6. Reflecting sidewalls.

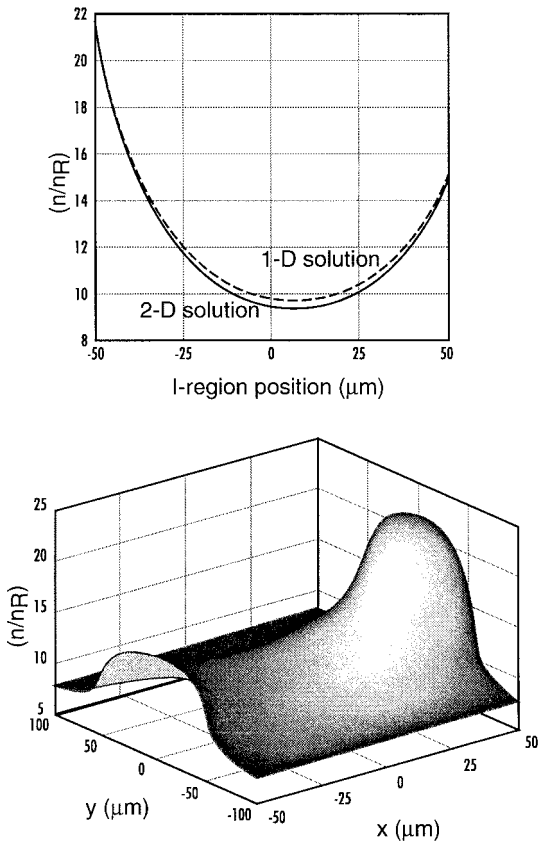

Fig. 7. Absorbing sidewalls.

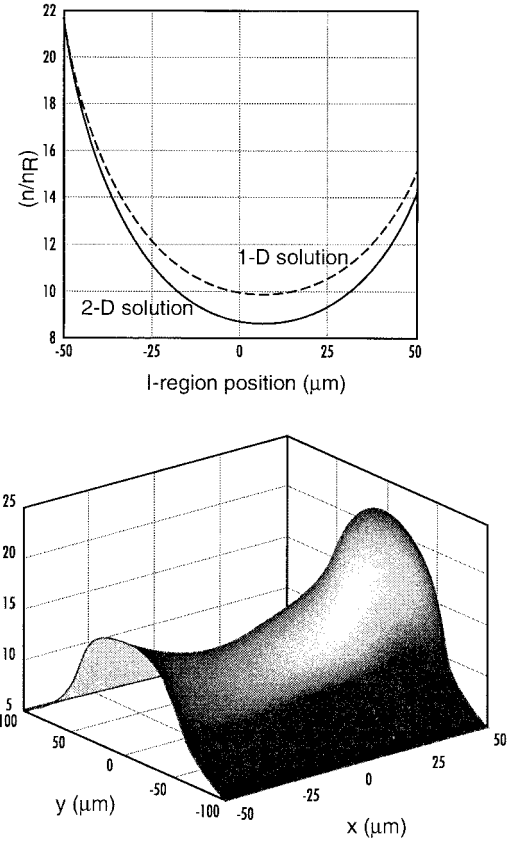

Fig. 8. Absorbing sidewalls, narrow device.

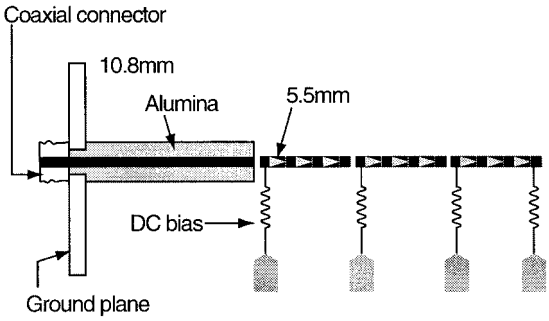

Fig. 9. Assembled monopole unit. It consists of four regions, one metal on alumina and three identical plasma islands. The assembly includes all the required biasing and filtering.

tion in carrier density. All of the applied current basically goes into surface recombination currents.

We conclude that either we have low surface recombination at the sidewalls or that the sidewalls are at a considerable distance from the main flow of carriers, i.e., diode width must be significantly greater than the contact width.

Several important predictions resulted from the simulations.

- Injected carrier densities in the range we need (10^{18} cm^{-3}) can be realized with short "I" layer lengths at or below 100 μm.
- Isolation trenches can be tolerated even if they have high surface recombination and if the walls are greater than 50 μm away from the active device channel.

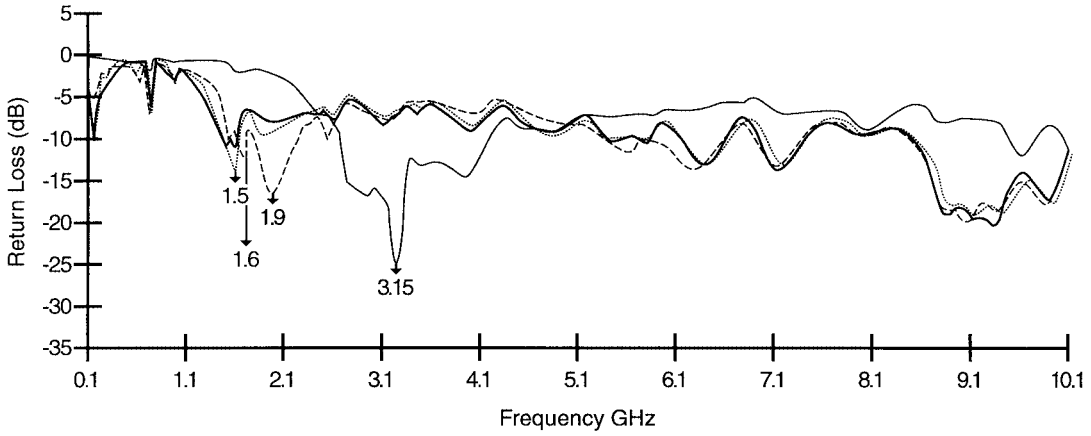

Fig. 10. Measured return loss in decibels of the assembled monopole at four different bias settings. The performance demonstrates frequency-hopping operation.

- Increasing the injection currents beyond what is necessary for plasma densities around 10^{18} cm^{-3} will cause additional thermal load without increasing the "I" layer plasma density.
- Deep drive-in of the n^+ and p^+ contact regions is undesirable because it can result in back injection of carriers into the deep lower doping concentration areas.
- There is a strong dependence of the effective diffusion length on the carrier concentration level. Thus, for given required carrier concentrations, the diffusion length limits the maximum length of the I-region, without considering the effects of any recombination. This analysis showed that the length of the "I" layer must be in the range of 100 μm.

These idealized simulations also identified several important design constraints. First, the high dc injection level drives the carrier recombination, and the carrier recombination places a limit on the length of SPIN device for carrier densities of 10^{18} cm^{-3}. Since the high injection level drives the recombination mechanism, if the "I" layer is much longer than approximately 100 μm, pumping more carriers into the device is not of much benefit. Secondly, the sidewalls are sites for carrier recombination. This recombination at the sidewalls can be tolerated as long as the sidewalls are at least 100 μm away from the central axis of the device. This conclusion leads us to a device layout that has rather narrow contacts (approximately 50-μm wide) with sidewall trenches at least 100 μm away on either side. The derived optimum device geometry has been utilized in the following proof-of-concept experiments.

III. Monopole Antenna Proof-of-Concept Experiments

A few basic questions needed answers before we could implement this approach. These questions included: Do the plasma islands radiate? Can we use these antennas to demonstrate the antenna's reconfigurability? And most importantly, what is the efficiency of these radiators?

To answer these questions and concerns, we have selected the hologram's basic building block, the dipole, and we carried out a few experiments to investigate the feasibility of this approach. For structural simplicity, we have used a monopole antenna structure as our first vehicle for validation and demonstration experiments.

First Experiment: An antenna structure was assembled using SPIN devices with a 500-μm I-region length utilizing a bonded wafer. Fig. 9 shows the assembled monopole structure. We have demonstrated the antenna's reconfigurability by turning ON or OFF various sections, to change the active length of the assembled monopole antenna structure. As expected, as more sections are turned ON, the operating frequency shifts to lower values. Typically the monopole (if all sections are OFF) operates at 3.25 GHz. When the first section is turned ON, the operating frequency shifts down to 2 GHz. This can be demonstrated by measuring the return loss of the monopole antenna under different bias conditions (as seen in Fig. 10), where the match at 2 GHz is now significantly enhanced. Similarly, by turning ON the second and third sections of the assembled monopole structure, the operating frequency shifts further down to 1.6 and 1.5 GHz, respectively. This frequency-hopping operation is one approach to reconfiguring the antennas.

Does this match enhancement reflect better antenna efficiency or it is merely the result of more absorption? To answer this, we measured the transmission coefficient (in the near field) between two similar monopole antennas. We connected two similar monopole antennas to ports 1 and 2 of a network analyzer. A significant increase was noticed in the transmitted power between the two similar antennas when similar sections are turned on. The significant increase in the transmitted power is a good indication that the enhanced match demonstrated at the monopole operating frequencies correlates to better radiation efficiency without more absorption.

We also have measured the monopole antenna radiation pattern (Fig. 11) at various operating frequencies They are typical of those of a monopole antenna with a finite ground plane. Effects of bias lines and bias-line filtering were carefully monitored to validate that the source of this radiation is definitely the plasma region (the monopole region) and not, for example, the bias lines.

Second Experiment: Our second experiment was very similar to the first, except that we used devices with shorter length (200 μm) and much wider width (1500 μm) I-regions to build a dipole antenna on a bulk wafer. The dipole has five sections that are switched ON by SPIN devices (see Fig. 12).

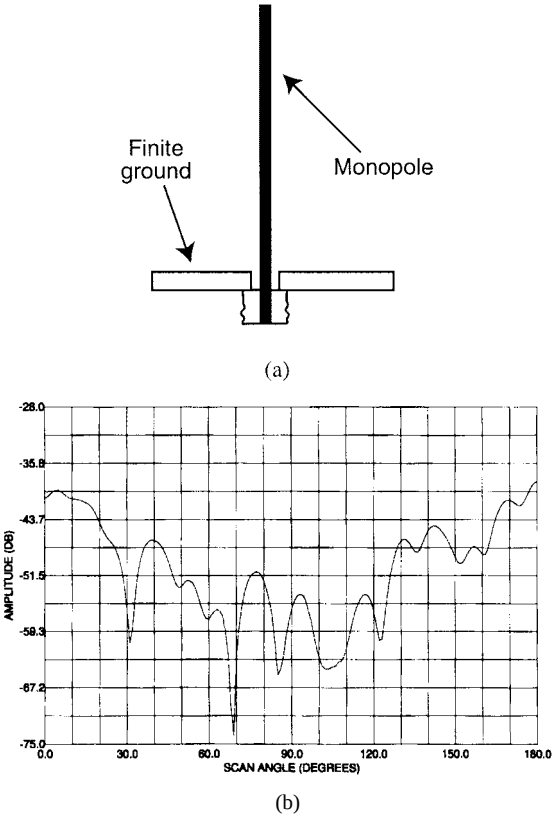

Fig. 11. (a) Monopole antenna on top of a finite ground plane. (b) Measured radiation pattern.

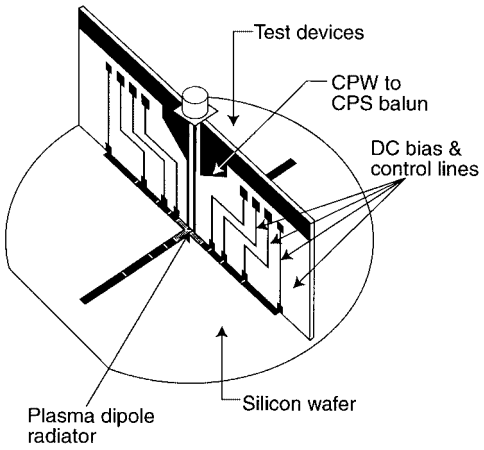

Fig. 12. Monolithic dipole on a silicon wafer. The SPIN devices here have 220-μm I-layer long. A balun was used for an RF feed.

The measured return loss in the ON and OFF states indicate resonance of the dipole elements are enhanced when their corresponding sections are activated. The radiation pattern of the assembled dipole was measured and calibrated against a copper dipole reference version. The radiation patterns were very similar, and the gain of the plasma antennas was approximately 10 dB below that of the copper version (see Fig. 13). Using a bulk wafer did not lead to a high carrier confinement near the surface.

Therefore, we repeated the same experiment using optimum devices with a shorter I-region length of 140 μm. This new device geometry is based on recent investigations of the device

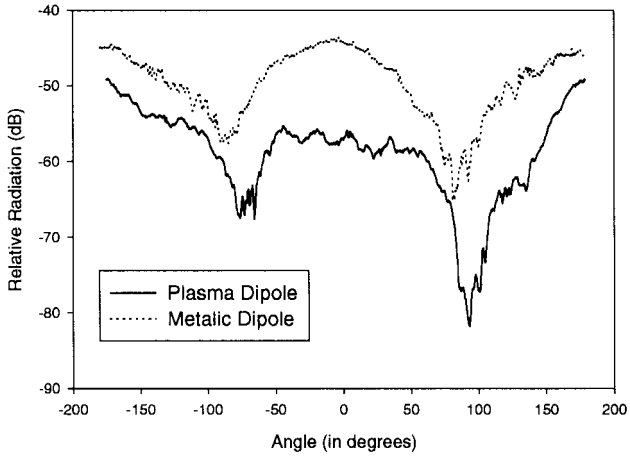

Fig. 13. Radiation pattern of the dipole antenna fabricated on the bulk wafer. The radiation pattern is for a dipole plasma antenna under dc control compared to a reference metallic dipole.

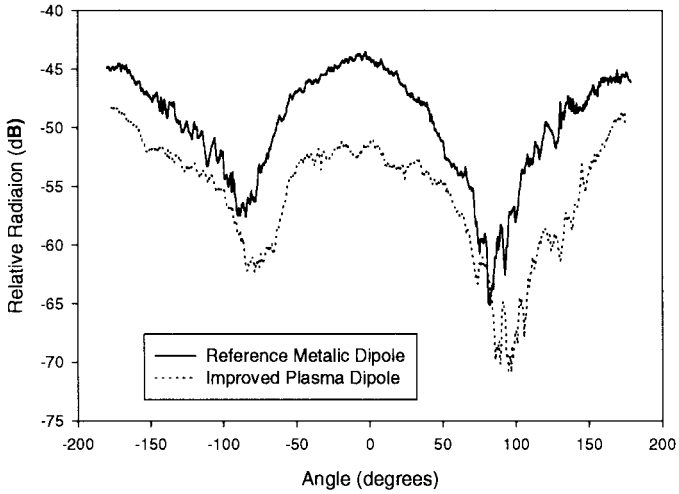

Fig. 14. Radiation pattern of the improved dipole antenna measured and calibrated against that of the reference copper dipole.

geometry previously outlined where we have also used bonded wafers to enhance the carrier concentrations in the SPIN device defined channels.

The radiation pattern of the assembled dipoles was measured and calibrated against that of the reference copper dipole. The radiation patterns were again very similar, and the gain of the plasma antennas was only 4 dB below that of the copper version (see Fig. 14). This relative improvement in gain performance is related to the use of metal-like plasma islands with relatively higher conductivity compared to that of the first assembled dipole antenna with the 220-μm I-layer. This wafer with the 140-μm I-layer also has better carrier confinement than that of the 500-μm I-layer that was used in Experiment 1. However, higher carrier confinement is still anticipated with further processing developments.

IV. Practical Implementation of the Reconfigurable Monopoles

What is the practicality of this approach? To answer this question, we need to discuss different issues, including dc power

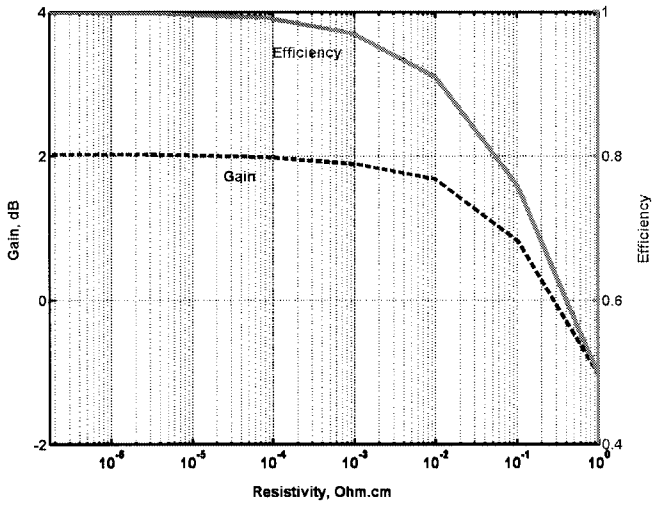

Fig. 15. Effect of dipole metallic resistivity on the gain and efficiency of a half-wavelength dipole antenna.

consumption and effects of the bias arrangement on the RF performance. For a device with a 140-μm I-layer, we need approximately 20 mA and 1 V to turn each junction (SPIN device) on. Hence, for an X-band ($\lambda/4$) monopole, we need roughly a 20-mm length. This is approximately equivalent to 70 junctions. Hence, it would require 70 V to turn the devices ON (if junctions are connected in series for example) and approximately 140-mW dc power dissipation for the whole antenna. Obviously, dc power dissipation is significantly reduced when operating at higher frequencies.

Metallization conductivity affects the antenna gain and efficiency. In general, metallic wire antennas' gain and efficiency η are slightly affected by the type of metallization used in their fabrication. Here is an example of a dipole antenna at 10 GHz (shown in Fig. 15, and Table III), where the gain and efficiency (η) are given as a function of their bulk resistively.

In Table III, we have utilized the following formula to calculate the overall antenna efficiency:

$$\eta = \frac{R_{\rm rad}}{R_{\rm rad} + R_{\rm ohmic}}$$

where $R_{\rm rad}$ is the radiation resistance of the antenna and $R_{\rm ohmic}$ is the ohmic loss resistance. Table III shows that if the antenna is made of copper, η is 99.9%; if it was made out of relatively lower conductivity material with $10^{-2}\ \Omega\cdot$cm, efficiency may dip well below 90%. Using a highly doped semiconductor material [11] with carrier concentration in the range of $> 10^{18}$ carrier/cm^3 will lead to an efficiency exceeding 75%. Carrier concentration of $> 10^{18}$ carrier/cm^3 levels is achievable, according to our SPIN device analysis. Based on our plasma dipole gain measured results, an estimate of 30%–40% overall antenna efficiency has been achieved, which translates to approximately a 10^{17} carrier/cm^3 carrier density. Also, from a dc power dissipation point-of-view, simple calculations (similar to those above) indicate that 4 W are required for an L-band dipole antenna, relative to 0.4 W for an X-band $\lambda/2$ dipole antennas. Hence, it is anticipated to dissipate relatively lower dc power when operating at higher frequencies.

V. Challenges and Limitations

Antenna Bias and Control: One of the challenges of the proposed concept is to design and fabricate a biasing arrangement that does not interfere with the RF operation of the antenna. A candidate design comprises thin conducting p-i-n's, embedded in a low dielectric-constant layer and directed to the semiconductor surface on the back side of the dielectric sheet. This arrangement takes advantage of the fact that the primary radiation field is polarized parallel to the antenna surface. Thus, vertically mounted p-i-n's will not substantially disturb the field. Moreover, in view of the fact that the surface wave field is highly localized near the surface, the biasing p-i-n's need not be long to avoid disturbance of the field by the ground plane. The p-i-n's are in contact with both the back terminals of the doped semiconductor regions and the control and addressing board through a set of bumps on both ends (see Fig. 2(b)). In other words, the bias p-i-n layer is sandwiched between the mounted semiconductor layer and the ground plane with the bias control board. The control board in turn is located on the backside of the ground plane.

In addition, the RF performance of the reconfigurable antenna configuration is influenced by several factors. In the following, we briefly address the main parameters, which have considerable effects on the antenna operation and, therefore, the antenna performance and limitations:

Wafer Size: It is obvious that the size of the antenna determines the lower frequency limit of operation. The practical size, determined by semiconductor processing technology, is a 6-in (or 150-mm) diameter. Therefore, a lower frequency limit of approximately 2 GHz is expected. This is roughly calculated as the longest half-wave dipole that can be accommodated on the wafer surface. If a high dielectric constant front sheet is used, this limit can be somewhat lower, as the resonant frequency of the dipole is reduced. Thus, the lower frequency limit is established basically by the technology of silicon processing.

At this lower frequency limit, the beamwidth attainable will be comparable to that of a dipole in free space. To generate narrow-band beams, the antenna size has to be larger relative to the free-space wavelength of the signal of interest. Therefore, the frequency of operation has to be higher than the lower limit, which is established only by antenna matching. This limitation can be alleviated if a multielement antenna configuration is used. The lower frequency limit, though, is maintained, as the individual elements have to still fit on a single wafer. Stretching the individual elements over several wafers (tiling), although theoretically possible, is not advisable in practice because of the discontinuities involved.

Solid-State Plasma Density: In general, the higher the semiconductor plasma density, the better the RF performance, as the conductivity of the material approaches that of a perfect conductor. However, an increase in the plasma density is at the expense of more dense location of the diodes and the applied dc-bias current. Thus, high-resolution addressing and higher drive power are required. The plasma density needed for satisfactory operation of the antenna is roughly determined by the skin depth of penetration of the RF field into the plasma regions. The longer the skin depth, the less the antenna's efficiency due to surface losses. Device simulations indicated

TABLE III
EFFECT OF RESISTIVITY ON ANTENNA PERFORMANCE

Resistivity (Ohm.cm)	Gain (dBi)	Conductor Loss (dB)	Efficiency	Comments
1.724E-7	2.02	0.01	99.9%	Copper
2.655E-6	2.02	0.01	99.8%	Aluminum
7.200E-5	1.99	0.04	99.2%	Steel
1.000E-4	1.98	0.04	99.0%	
1.000E-3	1.89	0.14	96.9%	
1.000E-2	1.68	0.41	90.9%	10^{19} cm^{-3} impurity concentration
1.000E-1	0.83	1.2	75.9%	
1.000E+0	-1.03	-3.06	49.5%	

that levels of 10^{17} to 10^{18} carriers/cm^3 are achievable with SPIN devices lengths on the order of hundreds of micrometers.

Thermal Considerations and Packaging: In view of the fact that there can be a considerable current drive in the semiconductor, leading to the dissipation of substantial amount of power, special care has to be given to the antenna packaging and the materials used. High thermal conductivity and low RF dielectric loss are required as the carrier sheet for the silicon wafer. Moreover, the sheet has to match the silicon material in thermal expansion to avoid cracking over the large surface of the antenna. Aluminum nitride, for example, appears to be a good candidate for use in the proposed configuration.

VI. SUMMARY AND CONCLUSIONS

The innovative reconfigurable aperture antenna concept represents a qualitative advancement compared to the state-of-the-art. This concept allows a great deal of operational flexibility. In the last few years, antennas utilizing somewhat similar concepts have been developed, with conductive patterns formed by optical excitation of semiconductors. Although the basic concept is similar, the implementation is quite different. Optical excitation is plagued by a number of serious problems, resulting in high-risk and high-cost devices. Excessively high optical power levels combined with the need for high resolution and high contrast irradiation create difficult problems for such an approach.

Our novel approach uses junction carrier injection in high-resistivity silicon, requiring much lower power levels and less expensive sources. In comparison to the optical excitation, our approach allows for a much more direct interface to the external feed circuitry, an important factor for the practical implementation of the reconfigurable antenna. In addition, high resolution can be obtained since very small features in semiconductors are continually produced.

The feasibility of the plasma antenna has, of course, depended on the possibility of creating sufficiently conductive patterns on semiconductors. It has been demonstrated that carriers in semiconductors form plasma, which at high enough levels causes the semiconductor to behave as a metallic medium. We have achieved carrier density levels on the order of 10^{17}–10^{18} cm^{-3} through special processing techniques and carrier confinement channels. We have optimized the SPIN device configuration to confine the plasma domains to the surface of the antenna aperture. Plasma radiators have been fabricated and their radiation patterns measured. Further processing improvements are necessary to increase the carrier confinement and isolation of the SPIN devices. We have also demonstrated the use for this new technology for reconfigurable antennas by highlighting the monopole/dipole antenna experiments. We believe that, following improvement of the device characteristics, this technology shows feasibility and promise for use in adaptive and reconfigurable antennas.

The reconfigurable antenna investigated here can be used in several different modes. Thus, planar-type radiators akin to Yagi-type antennas can be used at relatively low frequencies. Volume-type antennas, including the holographic type, can be used at higher frequencies. In all modes, the reconfiguration feature can be used to either optimize the antenna performance at a given frequency or change its parameters electronically (e.g., beam steering and frequency hopping).

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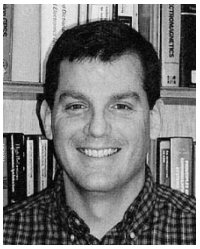

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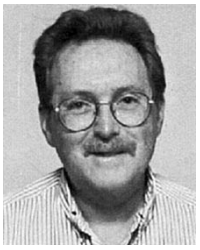

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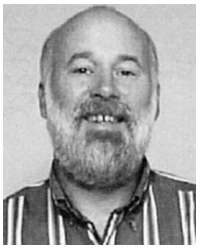

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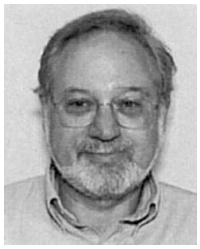

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